Small Via High Aspect Ratio Circuit Edit: Challenges, Techniques and Developments

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Abstract

As semiconductor device manufacturing technologies move below the 100 nm node constrains on using Focused Ion Beam (FIB) systems to perform circuit edit operations tighten dramatically. Phenomena associated with via milling and deposition processes, considered minor side effects in the past, may become performance-limiting factors.

Obstacles, associated with editing deep sub micron technologies beyond 100nm node, which include navigational accuracy, beam placement stability, and small via milling and filling processes, cannot be completely overcome without advances in overall FIB system performance and operation.

We present a detailed technical overview of the challenges, associated with silicon microsurgery on devices, manufactured with sub 100 nm process technology and describe recent advancements in FIB technology and techniques which address these areas and allow successful modification of today's most advanced designs.

Introduction

Circuit edit – the modification of integrated circuit (IC) devices at the interconnect node level – has for many years been an important part of the product introduction process for IC manufacturers. By validating proposed design changes and producing prototype parts for downstream, FIB can significantly shorten new product introduction cycles in addition and to market for product improvements.

For FIB circuit edit to maintain its utility in this role, it must overcome significant challenges posed by shrinking geometries, higher clock speeds, changes in materials and increase in number of interconnect layers.

All FIB circuit edits require certain steps in the process. First, the beam should be accurately positioned over the target line, then an access via should be drilled to the target, and finally the target line is cleanly severed or an electrical connection to the line is made.

Decreasing device dimensions require improved stage and beam positioning accuracies in order that a milled via contacts the intended line. For the majority of high-end devices this navigation must be done "blind", since devices either are buried beneath the silicon substrate or are completely planarized. Such "blind" navigation is achieved by establishing a "lock" – coordinate transfer function between the CAD layout of the IC and actual coordinates of the device on the stage of the FIB system.

As the IC manufacturing technology progresses beyond the 100nm, it could become critical to allow and compensate for the effects of die distortion caused by the packaging process. Use of computer intelligence and automation of locking techniques could eliminate operator-related errors and improve the accuracy of locking.

Once the beam is positioned over the target, access via is milled through the substrate to the target metal line. The mill must be stopped when the line exposures, without affecting neighboring structures. The ion beam current used for milling is steadily decreasing, as it becomes necessary to mill smaller and smaller vias. In order to accurately endpoint during such mills improved signal collection and detection is needed.

Application of the FIB edits to a validation of dynamic performance of the device (as opposed to a static logical validation) could be more effective, if parasitic resistance and capacitance of the edit will closely approximate such values of the fabricated line. Accomplishing this task would be easier with lower resistivity conductor and lower leakage dielectric materials, than are currently offered by most common FIB deposition processes.

This paper describes recent improvements in all of these areas: navigation, milling, deposition, and endpointing that enable FIB circuit editing on sub-90nm devices.

Navigation

A process of editing the integrated circuit, either from a back side or a front side, beings by navigation to the area of interest. Precision navigation is achieved by correlating reference marks, physically on the device and in the corresponding CAD database, and performing "CAD to FIB lock" – conversion of the CAD coordinates to the coordinates of the device in the FIB system.

After the lock has been established, multiple factors, which affect the ultimate accuracy of the positioning, should be taken to account. In addition to the well-understood issues of thermal drift, "Cosine" and "Abbe" [1] errors which are addressed by the calibrations and mechanical hardware of the stage, number of FIB-specific and IC-specific factors, such as beam drift, sample charging, lithography misregistration and die distortion during the packaging of the IC should be taken to account.

In order to achieve the navigational accuracy, necessary to work with devices below the 100nm node (Fig. 1), a number of advanced technologies should be employed. One such technology uses laser interferometer to guide the stage. After stage reaches the required position and stops, feedback from the interferometer is used to actively correct for drift and residual errors by deflecting the beam to cancel the drift.

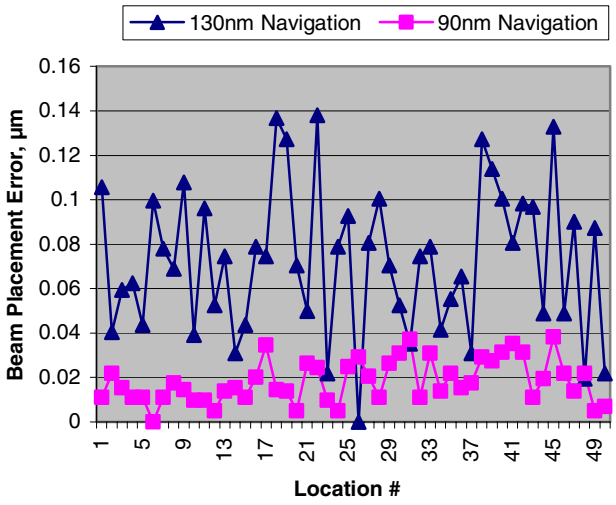

Fig. 1: Positioning errors, characterizing improvement of beam placement accuracy from 140nm to below 40nm p-p. The data is collected by navigating in a random order to the known locations on the packaged die, both before (130nm navigation) and after (90nm navigation) the application of laser error compensation, enhanced lock algorithm and stage mechanism improvements.

While the resolution of the laser interferometer can reach fractions of a nanometer and the achievable accuracy of the interferometer-based position feedback system well below 10nm is possible [2], some of the IC-specific sources of the navigational errors remain and should be compensated.

One of the other technologies, employed jointly with the laser interferometer-based error compensation, is the enhanced lock algorithm with compensation of the die Z distortion and orthogonal errors. The algorithm improves the accuracy of the beam placement over the elements within a packaged die of the IC and helps to enable blind CAD navigation on devices below 100nm node.

It has been reported in the literature [3-5], that the die of modern integrated circuits may become distorted during the packaging process. While exact details of the X – Y distortion are very complex and not yet well understood, distortion of the die in the Z direction can be measured directly. Multiple methods to characterize Z distortion can be proposed, including direct Z measurements of polished die by an IR microscope and surface profile scanning by a laser profilometer. We are evaluating both methods using in-situ IR microscope and data collected from scanning the die by an interferometer-based surface profiler from the STIL Company. Both methods, applied to ICs with the significant Z distortion, yielded similar results and confirmed that the circuitry plane of the die deviates substantially form the leveled surface (Fig. 2). As the result of this deviation, X – Y positions of the sites within the die differ from the positions predicted by purely linear transformation of the CAD coordinates.

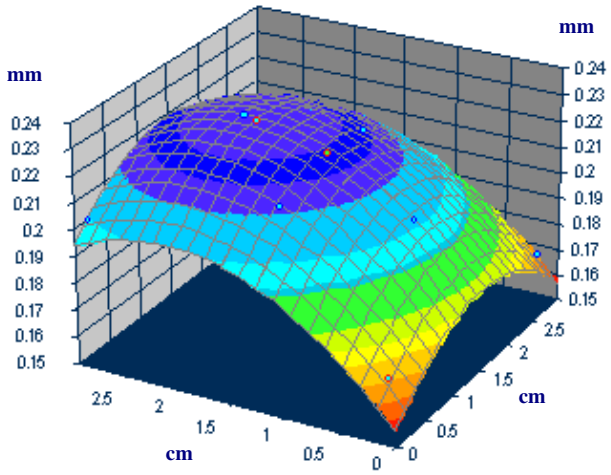

Fig. 2: Profile of the packaged die, reconstructed from limited number of data points, which were extracted from the die profile generated by laser interferometer.

After the deviation of the circuitry plane from the leveled surface is estimated, X – Y corrections for each particular

location on the die can be derived. Our model predicts a functional correction of up to more then 200nm in X-Y plane within the 25mm X 25mm die with a 100µm of Z distortion.

Currently, creating a "lock" between the CAD database and the device coordinates in the FIB involves manually associating locations within the CAD layout with positions on the device. Because of the variations in IC fabrication process, as well as the destructive effects of FIB imaging, the device structures in the FIB image and in the CAD database may vary, particularly in edge definition. Manual identification of the center of a particular device structure in an FIB image is tedious and susceptible to human errors. We estimate the uncertainty of location identification by operator to be at least ± 52nm, or ± 2 pixels assuming Field Of View (FOV) 20µm and image size 768X768 pixels, just due to the digital nature of the FIB image. While this manual method has been utilized successfully for some time, smaller device structures require defining edit locations more precisely.

Utilizing machine vision technology for pattern recognition (Fig. 3) on the associated CAD and FIB image areas, we are able to use sub-pixel interpolation and locate the lock structure with the greater accuracy and repeatability. In addition to improved accuracy, use of "computer intelligence" for navigation automates the process, thus making operating FIB system easier and improving consistency of the results.

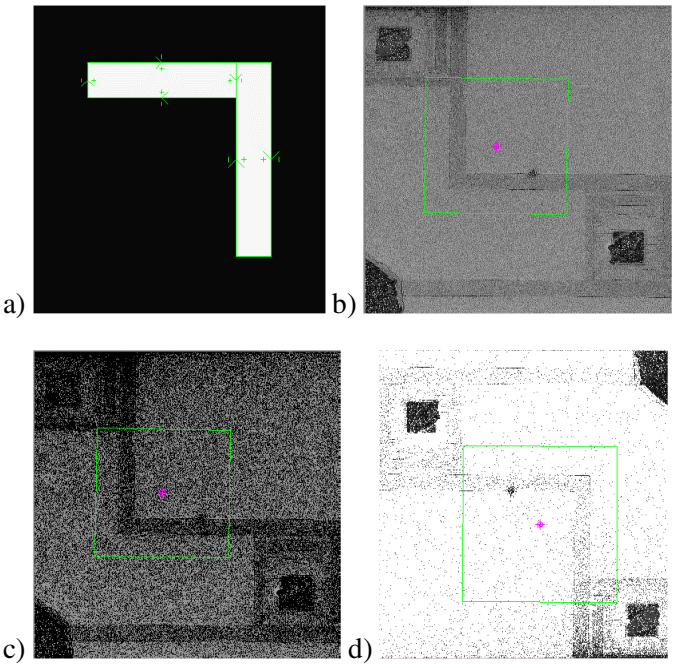

Fig. 3: CAD polygon pattern (a) is successfully recognized by the computer on the FIB images despite of low contrast (b), high noise level (c), and excessive brightness (d) conditions.

Extending the application of this pattern recognition technology will allow us to automatically compensate for beam placement instabilities that are inherent to the process of circuit editing in an FIB system, but cannot be tracked and compensated by the laser interferometer-based position feedback. Utilization of a reference structure, deposited on the surface of the sample in close proximity to the edit area, will allow automatic correction of drifts associated with beam stability, thermal expansion of the sample and surface charging, and improve beam placement stability during the repair.

Via milling and material deposition

Opening vias in a semiconductor device requires some indication of the depth and/or material being milled. Until recently, the most common technique to detect material change during the mill progress in a FIB system is through secondary electron endpoint.

Secondary electrons, along with the secondary ions, are generated by ion beam interaction with the sample material during the FIB milling process. Detection of the secondary electrons requires application of a positive bias to the detector. In this situation, the secondary ion information is rejected (Fig. 4) due to charge discrimination. Some small fraction of the secondary electron signal is also lost due to limited signal collection efficiency of the detector. As features shrink in size and via aspect ratio increase, the secondary electron signal becomes weaker and can eventually reach undetectable level.

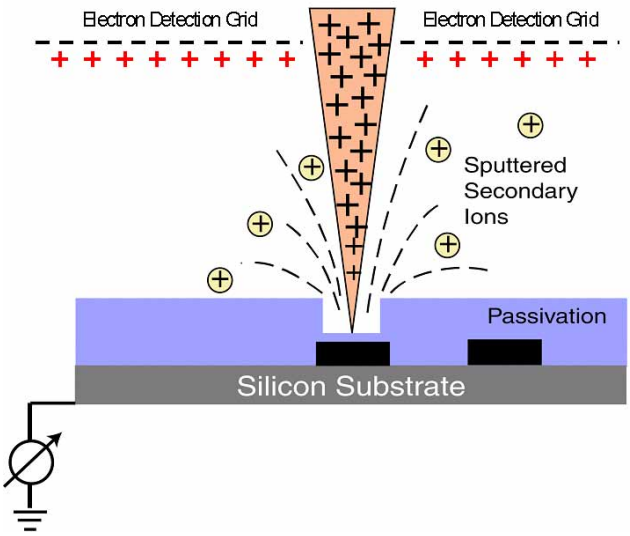

Fig. 4: Positively biased signal detector, used for secondary electron endpoint detection, is rejecting the secondary ion fraction of the endpoint signal.

Primary ion beam current together with the secondary electron and secondary ion currents define the bulk sample charging. Since in the generic case these currents are not balanced, the imbalance is compensated by the "sample-absorbed current" (or "stage current"), flowing between the sample and the grounded stage of the system.

The equation, describing the stage current, is $I_{SC}=I_{IB}+I_{SE}-I_{SI}$, where I_{SC} is the current flowing between the sample and the stage, or "stage current", I_{IB} is the primary ion beam current, I_{SE} is the secondary electron current, and I_{SI} is the secondary ion current. It is interesting to note that secondary electron and the secondary ion components of the equation have opposite signs and therefore the increase of the secondary electron current and/or decline of the secondary ion current will have same effect on the stage current, assuming that the primary ion beam current is remaining constant.

An experimental setup, based on a picoammeter with low noise and sub-Pico-ampere resolution and data plotting application created in TestPoint software, allows detecting distinct variations of the stage current and provides the operator with additional endpoint information. Via milling endpoint detection by monitoring the "stage current" graph is independent of the Field of View (FOV) of the FIB system.

A possibility to use the sage current plot for the via milling endpoint purposes was verified experimentally for vias as small as 0.3µm x 0.3µm and 5µm deep (Fig. 5), and found useful in both front and back side circuit edit applications.

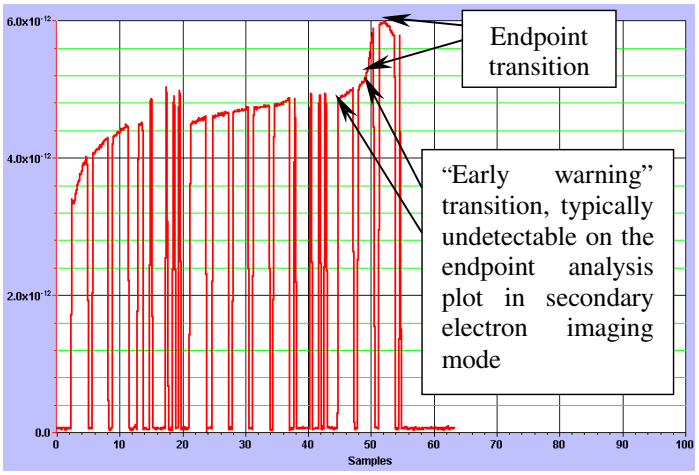

Fig. 5: Typical shape of the plot on the stage current monitoring setup, associated with the via milling endpoint detection.

Monitoring the stage current plot during the deposition process was also attempted and found useful for providing information about the via fill endpoint (Fig. 6).

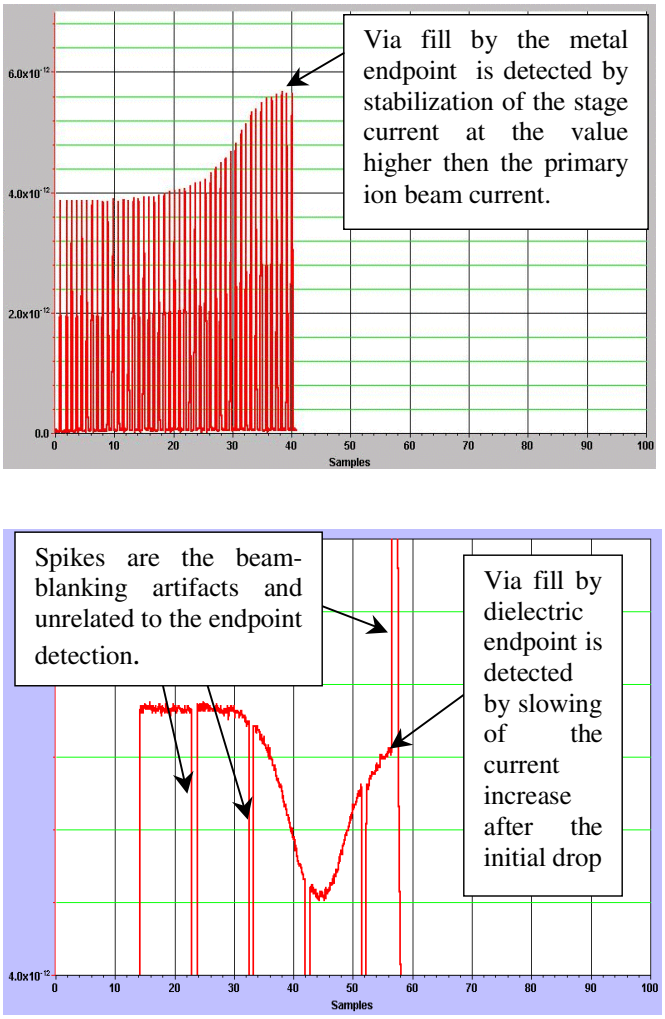

Fig. 6: Typical shape of the stage current plot at the endpoint of the via fill by FIB metal (a) and dielectric (b) deposition processes.

Via fill with metal was monitored by a stage current setup and the endpoint is determined when the stage current saturates at the value higher then the measured incident beam current. This indicates that the via is completely filled with metal and making a contact through the via, or else there will be no increase of the current.

Stage current endpoint of the via fill by dielectric is detected by slowing the increase of the stage current after the initial drop before the end of the via filling process. Accurate endpoint of the dielectric via fill during the backside edit process prevents buildup of the dielectric pillars due to deposition overdose.

Further development of the stage current endpoint methodology and possible use of digital signal processing for the real-time analysis of the data could offer a potential for the automation of the via milling and deposition processes.

Shrinking layout dimensions of the modern device interconnect creates increased aspect ratio of the access vias. While milling of High Aspect Ratio (HAR) and Ultra High Aspect Ratio (UHAR) vias by low beam currents was reported by FEI and others [6 and elsewhere] in the past, material deposition within the via remains a critical issue [7-9].

Existing circuit edit applications, and more than ever applications below the sub 100 nm node, could benefit from increased resistivity of the SiO_2 dielectric deposition.

Controllable parameters, affecting deposition of dielectrics in the FIB system, are the pressure of siloxane and oxygen precursor gases and the ion beam raster parameters, such as pixel spacing and beam dwell time. By employing Design of Experiment (DOE) techniques, we examined the effects of these parameters within the operating range of the FIB system [10] on the resistivity of the FIB SiO_2 deposition.

Results indicate that beam dwell time has the most effect on the resistivity, followed by O_2 and Siloxane gas pressures respectively. Decrease of the pixel dwell time during the deposition raster and reduction of the siloxane gas pressure increases the resistivity of FIB dielectric, while increase of the O_2 pressure provides similar effect. By optimizing these parameters, dielectric structures with $\rho > 5E15$ μΩ·cm (Fig. 7) can be deposited consistently. There is an ongoing effort to characterize material composition of the deposited dielectrics and correlate it with the resistivity data.

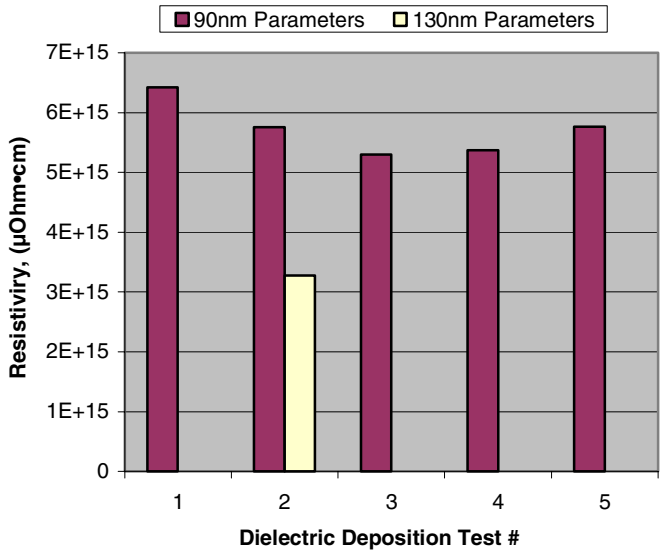

Fig. 7: Resistivity of the FIB SiO_2 dielectric deposition by "90nm optimized" parameters, compared to the best case of deposition with the "130nm standard" set of parameters.

Existing FIB-assisted metal deposition technology has been successful for device modifications over the last several years. Typical approaches deposit tungsten, platinum, gold, and other metals and achieve bulk material resistivity below 200 μΩ*cm [11, 12]. Inclusion of non-metallic atoms from the precursor, Ga implantation from the beam and non-crystalline morphologies of the deposition are the apparent reasons, preventing the achieving of lower resistivity values. Shrinking dimensions of the new semiconductor manufacturing technologies and the corresponding increase in speed of the IC operation require lower resistivity of conductive material to overcome the constrains imposed by a limited cross-sectional area of the HAR and UHAR circuit access vias.

We have investigated several alternative precursors and metal deposition approaches, which in most cases failed to provide improved resistivity over the existing tungsten deposition process. Tungsten by mesitylene tungsten hexacarbonyl ($C_9H_{12}W(CO)_3$) and aluminum by aluminum hexafluoroacetylacetonate ($Al(CF_3COCHCOCF_3)_3$, as well as tungsten hexacarbonyl in the presence of hydrogen as a reducing agent were tried over a variety of experimental conditions. In the case of the mesitylene tungsten hexacarbonyl material, very little data is available on its vapor pressure and we were unable to obtain a reasonable process pressure. The aluminum hexafluoroacetylacetonate material produced high rate depositions and yielded poor resistivities, probably due to large C and F inclusions. Tungsten deposited with hydrogen as a reducing agent yielded films of poor mechanical quality and no significant improvement in resistivity. Substrate temperature was varied over the range of about 25 to 100 °C for many of these experiments, with mixed results but never yielding both a good quality film and improved resistivity.

We have further developed a previously reported [13] method of FIB-induced deposition of copper-based metal films with resistivity well below 100 μΩ *cm for surface films (Fig. 8), providing a significant improvement over the presently available technology. Resistivity of the film strongly depends on the deposition growth rate, which must be well controlled to yield $\leq 0.2\mu m^3*nC^{-1}$ bulk material resistivity. Selecting beam raster parameters, the pixel spacing and dwell time, toward operation in a gas-depleted mode, controlled the growth rate.

We expect the FIB induced deposition process within the via be different from the deposition of the surface film due to restricted gas flow within the via. Therefore, the developed copper deposition technology will require further effort to characterize the resistivity of in-via deposition.

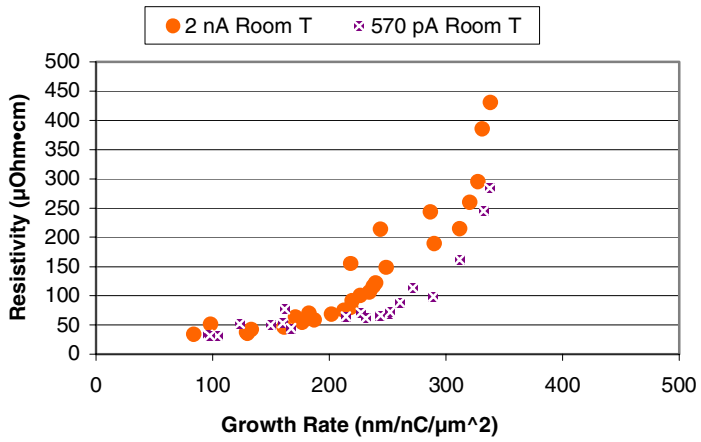

*Fig. 8: Bulk resistivity of the copper-based FIB conductor as a function of the deposition growth rate. Resistivity values well below 100 µΩ *cm were achieved at the practically viable deposition rates.*

Possible future trends of the technology

We believe that FIB Circuit Edit will continue to evolve with the progress of IC technology and remain a valuable tool for the device design verification for years to come. As semiconductor manufacturing will progress to ever-smaller dimensions below the foreseeable 50nm, difficulty of the circuit edit challenges will only increase.

Positioning challenges, associated with the navigation over the three-dimensional surface of the distorted packaged die would call for the beam positioning accuracy in single nanometer range. Such accuracy in conjunction with very small dimensions of the interconnect nodes, could require not only the ultra-precision stage navigation in X – Y plane, but also a real-time Z positioning of the die to maintain constant distance of the circuitry plane from the ion beam column and gas delivery system and provide necessary process stability. Novel chemistries and circuit edit techniques could be needed to address advances in materials and structures used in device manufacturing.

Requirements to the quality of the deposited materials will rise tremendously, as the cross-sectional area of the node access vias shrinks and volume of the in-via material reduces. Electron beam induced deposition of the Copper, reported [14] to attain material resistivity in 3.6 µΩ•Cm range at room temperature, could be the possible, but not the only solution to the problem of low resistance in-via deposition.

Electron beam induced deposition of dielectrics on the nanoscale level was reported elsewhere [15, 16]. Absence of the implanted Ga in E-beam induced dielectric deposition is expected to significantly improve dielectric properties of the materials for nanoscale depositions.

Further reduction of the ion beam currents, used for the ever smaller via milling and material deposition could require additional improvements in the imaging and detection and alternative or additional via endpointing techniques could become viable as the technology develops. One of possible candidates to provide additional material-related information during ion beam milling process is the Acoustic Ion Microscopy (AIM) [17]. The principle of AIM is baced on detection of the transitions in acoustic response of the sample materials to the ion impacts, similar to the Scanning Acoustic Electron Microscopy [18 - 20]. While typically reported lateral resolution of the AIM and SEAM techniques is in order of single micrometers, the depth resolution is not yet well understood. Short implantation depth (~30nm) of 50KeV Ga^+ ions and recent advances in the low level ultrasonic signal detection [21] could make acoustic techniques a promising direction for the advanced endpoint detection research. Multiple other approaches, including in-situ monitoring of the microwave resonant properties of the via being milled, could be proposed as an alternative or additional endpoint detection techniques.

Conclusion

We introduced a number of new technologies that will often be used for editing circuits with features smaller then 100nm. As the IC industry continues on the path set by Moores' law, not only is the fabrication of chips ultimately challenged, but also so are all of the testing and design verification activities.

We have identified and verified key technologies that will carry us into the near term future. These technologies are high accuracy X – Y navigation, precise endpoint techniques for ultra high aspect ratio via milling, low resistance metal deposition and high resistance dielectric deposition.

It is envisioned that FIB technology will continue to evolve and meet longer-term requirements. Changes in materials being used to fabricate ICs will require new processes and possibly new gas chemistries to be developed. Finally, endpoint techniques might require dramatically new technologies to detect material transition in vias with about 20nm opening.

Because of the tremendous value CE offers, companies will continue to develop technologies needed to overcome obstacles faced due to shrinking dimensions and material changes.

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